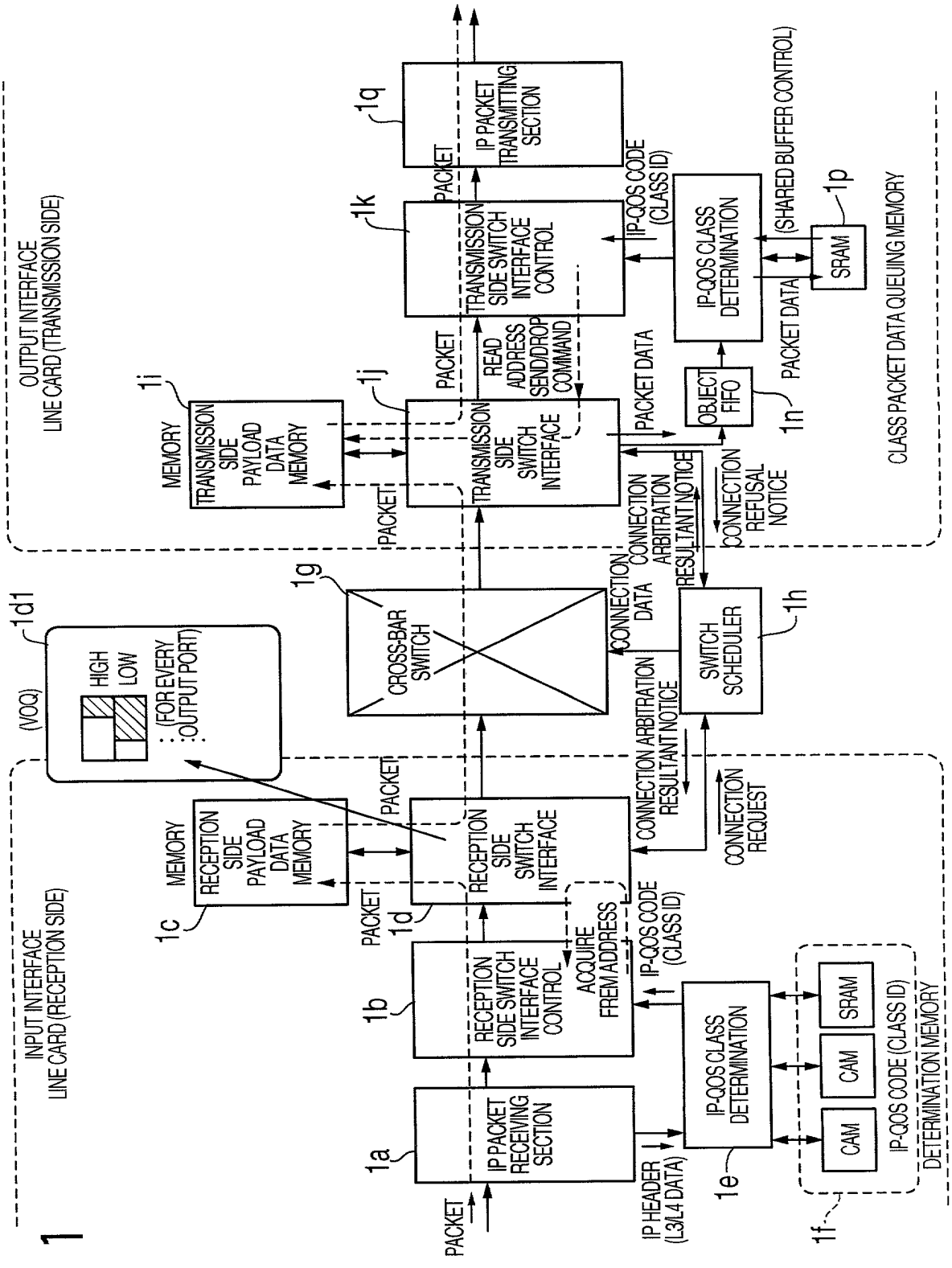

INPUT INTERFACE
LINE CARD (RECEPTION SIDE)
OUTPUT INTERFACE
LINE CARD (TRANSMISSION SIDE)
CLASS PACKET DATA QUEUING MEMORY
PACKET
IP PACKET RECEIVING SECTION
1a
RECEPTION SIDE SWITCH INTERFACE CONTROL
ACQUIRE FREM ADDRESS
1b
RECEPTION SIDE SWITCH INTERFACE
1d
MEMORY
RECEPTION SIDE PAYLOAD DATA MEMORY
1c
(VOQ)
HIGH
LOW
: (FOR EVERY : OUTPUT PORT)
1d1
IP HEADER (L3/L4 DATA)
IP-QOS CLASS DETERMINATION
1e
CAM
CAM
SRAM
IP-QOS CODE (CLASS ID)
DETERMINATION MEMORY
1f
IP-QOS CODE (CLASS ID)
CONNECTION REQUEST
CONNECTION ARBITRATION RESULTANT NOTICE
SWITCH SCHEDULER
1h
CROSS-BAR SWITCH
1g
CONNECTION DATA
CONNECTION ARBITRATION RESULTANT NOTICE
CONNECTION REFUSAL NOTICE
TRANSMISSION SIDE SWITCH INTERFACE
1j
MEMORY
TRANSMISSION SIDE PAYLOAD DATA MEMORY
1i
READ ADDRESS SEND/DROP COMMAND
PACKET DATA
OBJECT FIFO
1n
IP-QOS CLASS DETERMINATION
(SHARED BUFFER CONTROL)
SRAM
1p
TRANSMISSION SIDE SWITCH INTERFACE CONTROL
1k
IP-QOS CODE (CLASS ID)
IP PACKET TRANSMITTING SECTION
1q

Fig. 1

Fig. 2

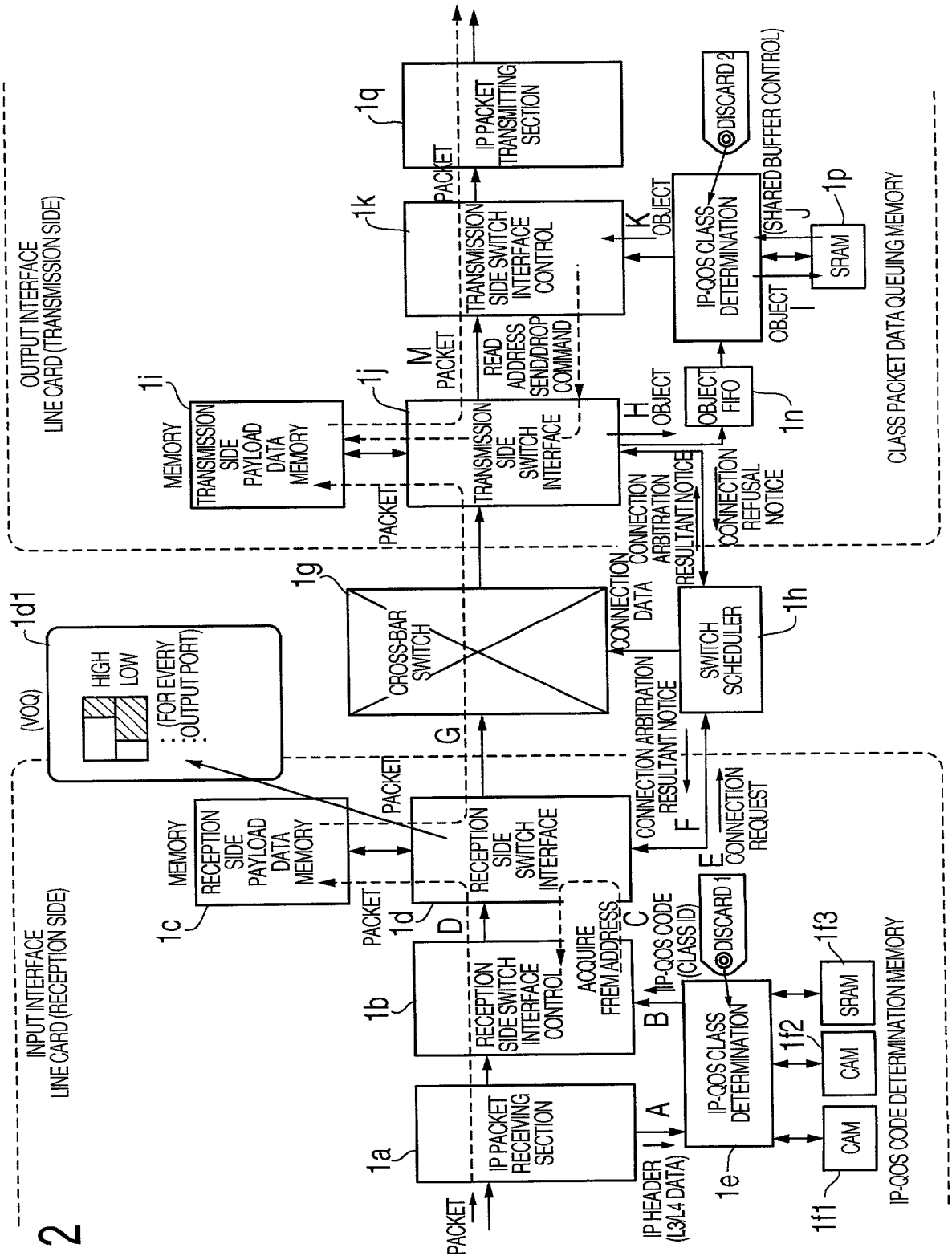


Fig. 3

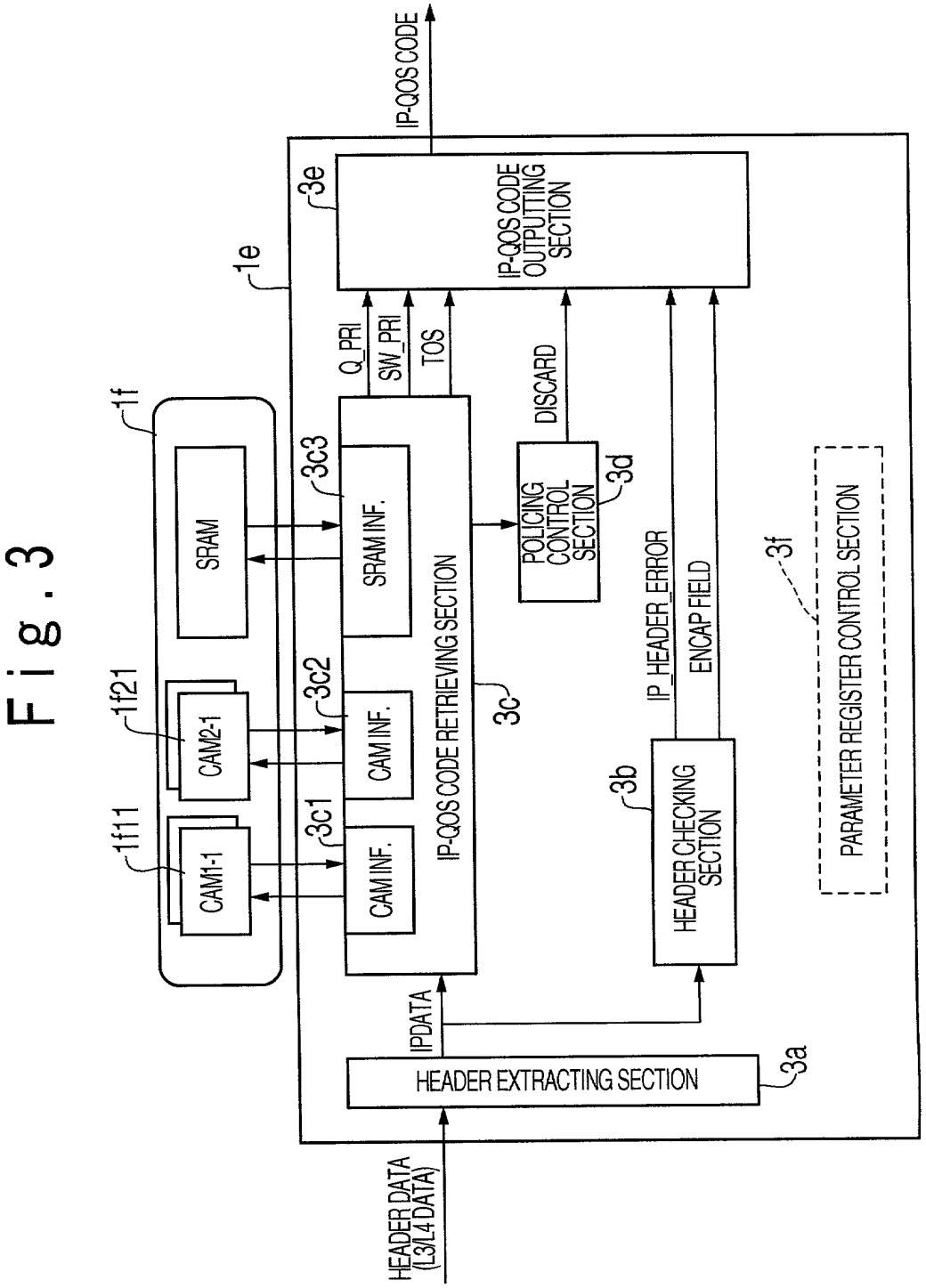

IP-QOS CODE
3e
IP-QOS CODE OUTPUTTING SECTION
1e
Q_PRI
SW_PRI
TOS
DISCARD
1f
SRAM
3c3
SRAM INF.
POLICING CONTROL SECTION
3d
1f21
CAM2-1
3c2
CAM INF.
IP-QOS CODE RETRIEVING SECTION
3c
IP_HEADER_ERROR
ENCAP FIELD
3f
1f11
CAM1-1
3c1
CAM INF.
3b
HEADER CHECKING SECTION
PARAMETER REGISTER CONTROL SECTION
IPDATA
HEADER EXTRACTING SECTION
3a
HEADER DATA (L3/L4 DATA)

Fig. 4

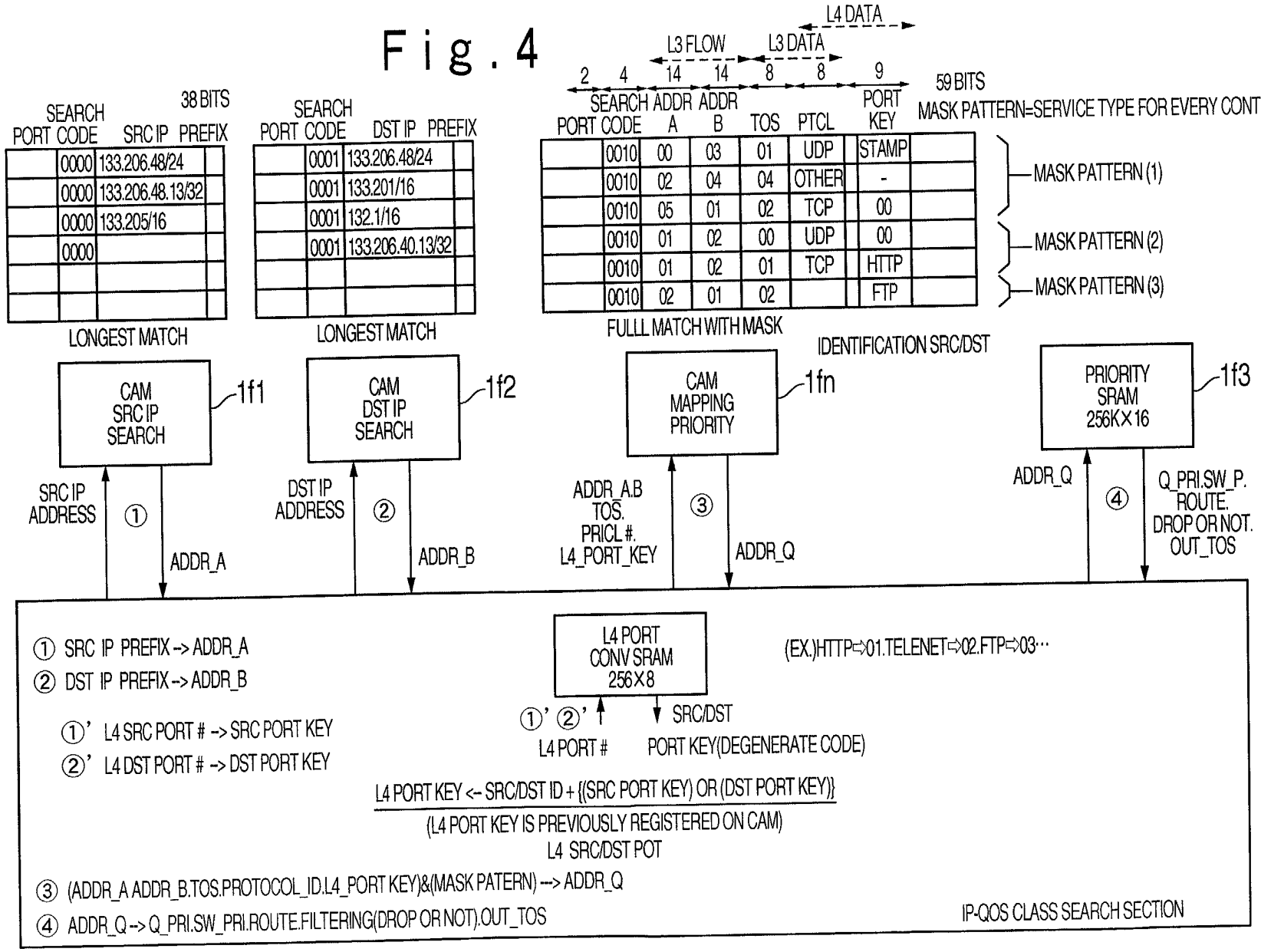


Fig. 5

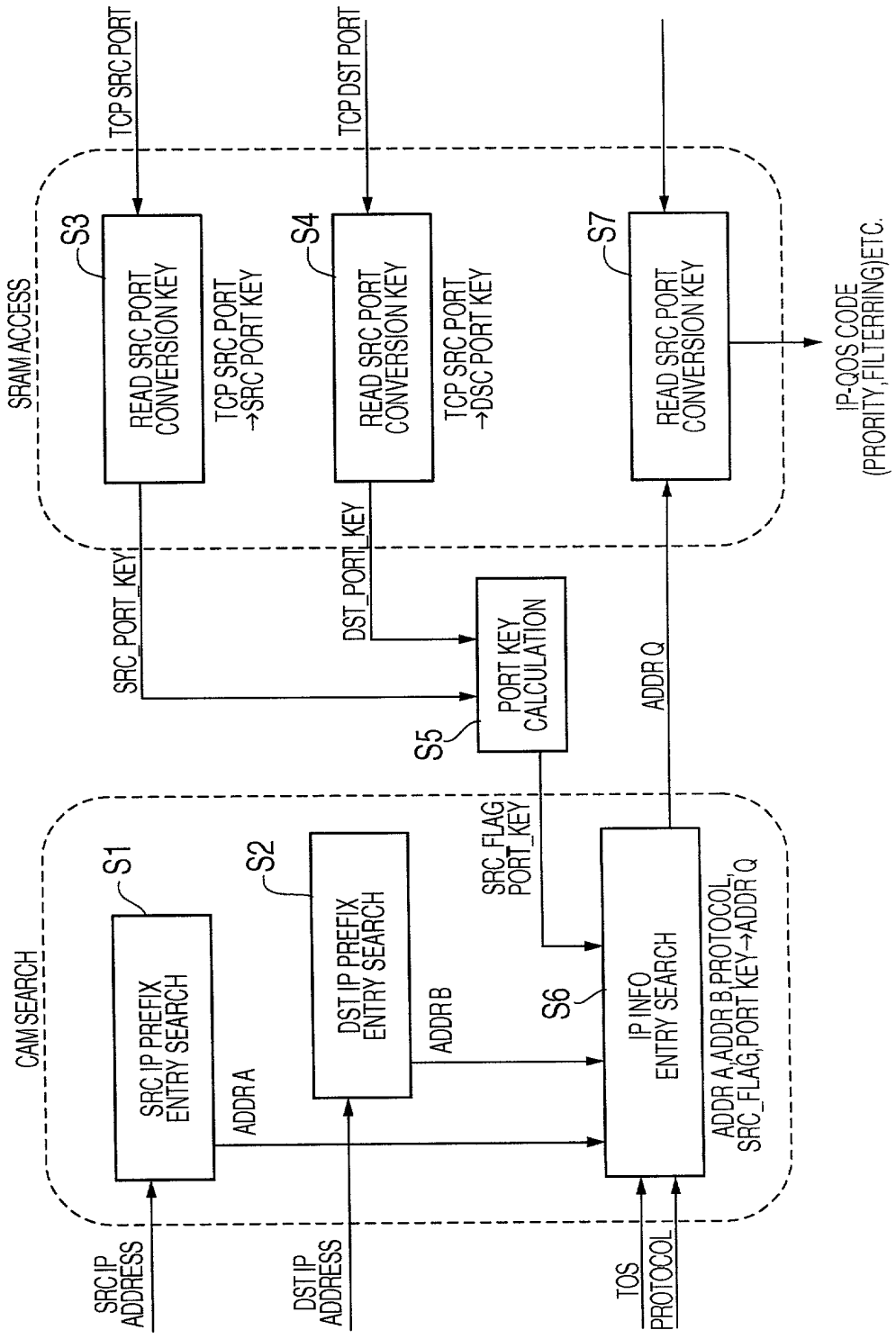

CAM SEARCH
SRAM ACCESS
S1
SRC IP PREFIX ENTRY SEARCH
ADDR A
S2
DST IP PREFIX ENTRY SEARCH
ADDR B
S3
READ SRC PORT CONVERSION KEY
TCP SRC PORT →SRC PORT KEY
S4
READ SRC PORT CONVERSION KEY
TCP SRC PORT →DSC PORT KEY
S5
PORT KEY CALCULATION
S6
IP INFO ENTRY SEARCH
ADDR A,ADDR B,PROTOCOL, SRC_FLAG,PORT KEY→ADDR Q
S7
READ SRC PORT CONVERSION KEY
IP-QOS CODE (PRORITY,FILTERRING)ETC.
TCP SRC PORT
TCP DST PORT
SRC_PORT_KEY
DST_PORT_KEY
SRC_FLAG PORT_KEY
ADDR Q
SRC IP ADDRESS
DST IP ADDRESS
TOS
PROTOCOL

Fig. 6A

【CAM REGION DIVISION】

CAM ADDRESS		CAM DATA (MAX.64 BITS)	MASK PATTERN (64 BITS)	SEARCH METHOD
	ADDR_A~	IP SRC PREFIX ENTRY STORAGE REGION		LONGEST MATCH
	ADDR_B~	IP DST PREFIX ENTRY STORAGE REGION		LONGEST MATCH
	ADDR_Q~	IP INFO SEARCH ENTRY STORAGE REGION		FULL MATCH WITH MASK

Fig. 6B

【1,IP SRC PREFIX ENTRY STORAGE REGION : SEARCH CODE 0000】

CAM ADDRESS (ADDR_A)	CAM DATA (38 BITS)			
	HW #(2)	SEARCH CODE(4)	IP SRC ADRESS/ PREFIX(32BITS)	NON USED(26 BITS)
A #1	00	0000	IP SRC ADDRESS #1/PREFIX	
A #2	00	0000	IP SRC ADDRESS #2/PREFIX	
A #3	01	0000	IP SRC ADDRESS #1/PREFIX	
⋮	⋮	⋮	⋮	

Fig. 7A

【2,IP DST PREFIX ENTRY STORAGE REGION : SEARCH CODE 0001】

CAM ADDRESS (ADDR_B)	CAM DATA (38 BITS)			
	HW #(2)	SEARCH CODE(4)	IP DST ADDRESS/ PREFIX(32BITS)	NON USED(26 BITS)
B #1	00	0001	IP DST ADDRESS #1/PREFIX	
B #2	00	0001	IP DST ADDRESS #2/PREFIX	
B #3	01	0001	IP DST ADDRESS #1/PREFIX	
⋮	⋮	⋮	⋮	

Fig. 7B

【3,IP INFO ADDRESS ENTRY STORAGE REGION : SEARCH CODE 0010】

CAM ADDRESS (ADDR_Q)	CAM DATA (55 BITS)								
	HW #(2)	SEARCH CODE(4)	ADDR A(14)	ADDR B(14)	TOS (8)	PROTO COL# (8)	SRC/ DST (1)	PORT KEY (8)	NON USED (5 BITS)
Q #1	00	0010	A1	B1	01	TCP	S	HTTP	
Q #2	00	0010	A1	B2	04	UDP	D	SNMP	
Q #3	01	0010	A3	B1	02	TCP	S	FTP	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

Fig.8

【IP INFO ENTRY】

ADDRESS(16 BITS) : UPPER 2 BITS=00 LOWER 14 BITS=HIT ADDR_Q	DATA(24 BIT)							
	Q_PRI(4)	D	P	ROUTE(1+4)		OUTPUT TOS(2+8)		RESERVE (3)
ADDR Q0	0000	0	0	0	0000	11	011011 00	
ADDR Q1	1101	0	1	0	0000	11	011010 00	
ADDR Q2	1101	0	0	0	0000	00	000000 00	
⋮	⋮	⋮	⋮		⋮		⋮	
ADDR QI	1110	0	1	1	0101	00	000000 00	
⋮	⋮	⋮	⋮		⋮		⋮	

Fig. 9

(IPV4 & TCP/UDP/OTHER HEADER FORMAT)

WORD	63			47	31			15
-	EMPTY DATA				PPP HEADER			
0	VER	IHL	TOS	DETAGRAM LENGTH	IDENTIFICATION		M	FRAGMENT OFFSET
1	TTL		PROTOCOL	HEADER CHECKSUM	SRC IP ADDRESS			
2	DST IP ADDRESS				L4 SRC PORT			L4 DST PORT

Fig. 10

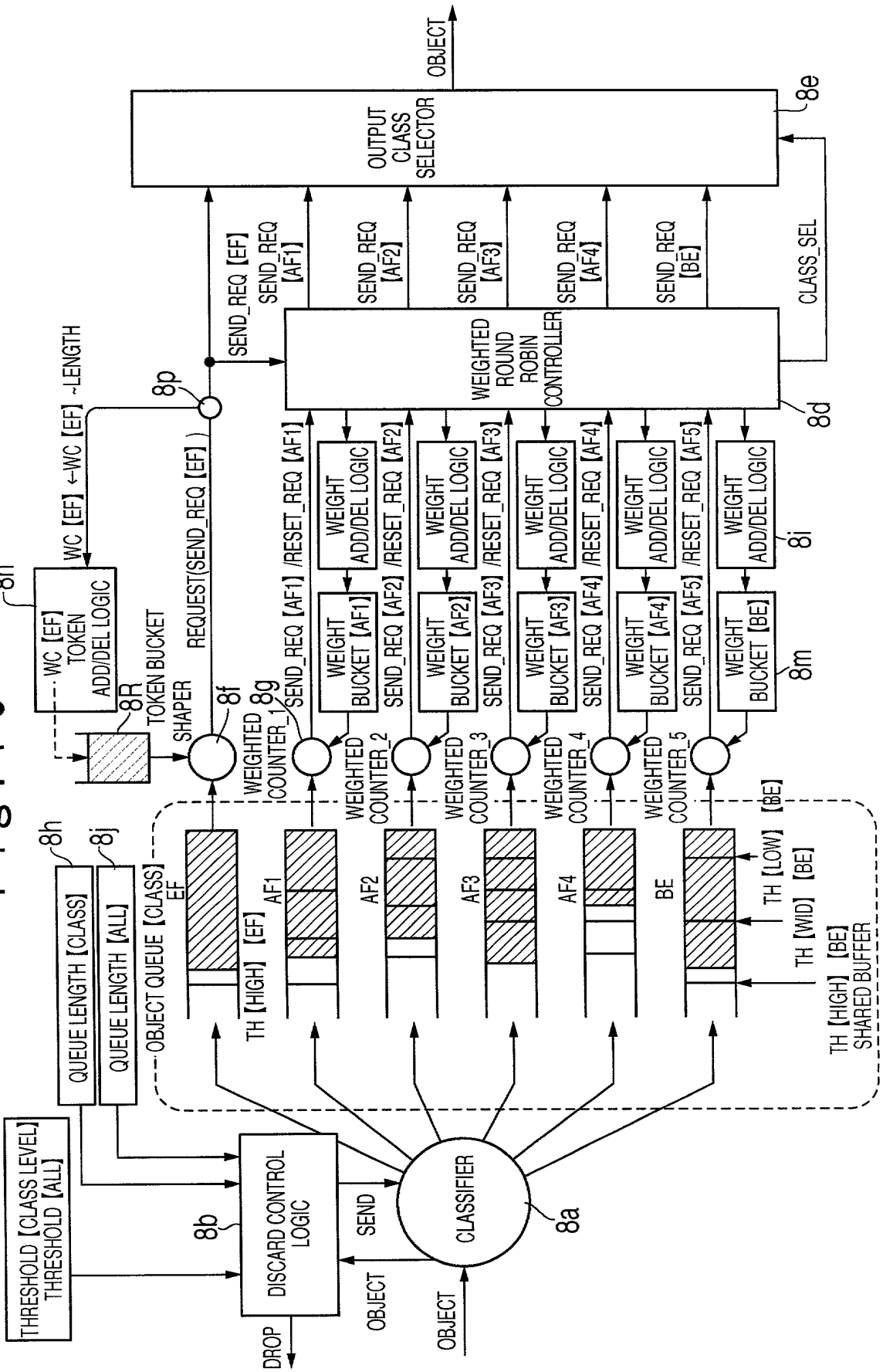


Fig. 11

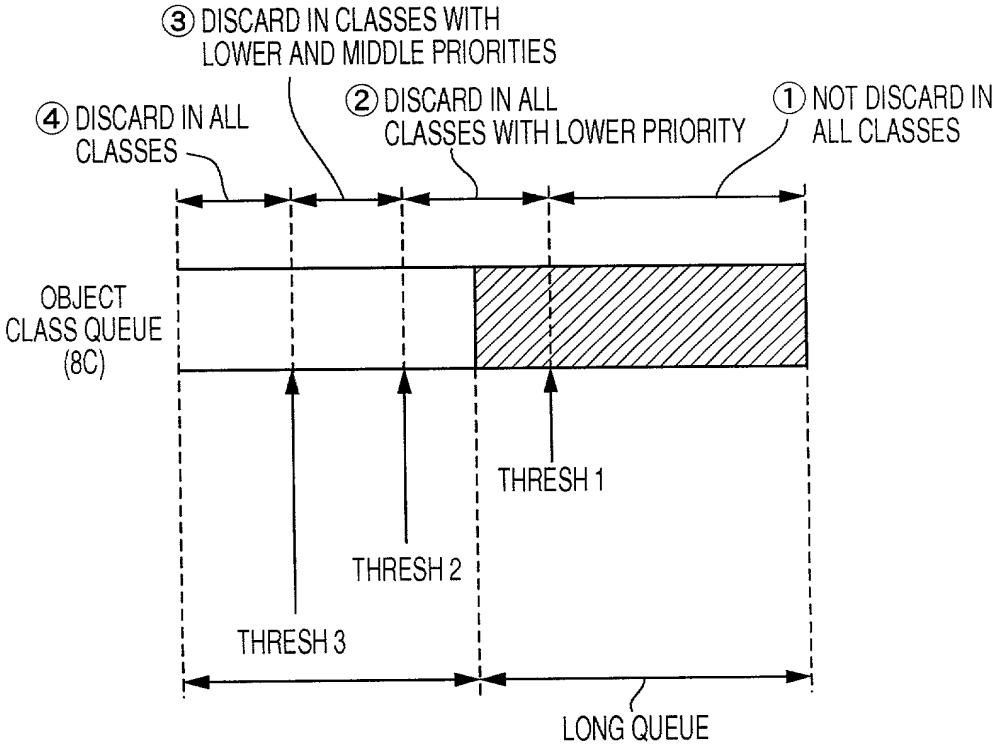

③ DISCARD IN CLASSES WITH LOWER AND MIDDLE PRIORITIES
④ DISCARD IN ALL CLASSES
② DISCARD IN ALL CLASSES WITH LOWER PRIORITY
① NOT DISCARD IN ALL CLASSES
OBJECT CLASS QUEUE (8C)
THRESH 1
THRESH 2
THRESH 3
LONG QUEUE

Fig. 12

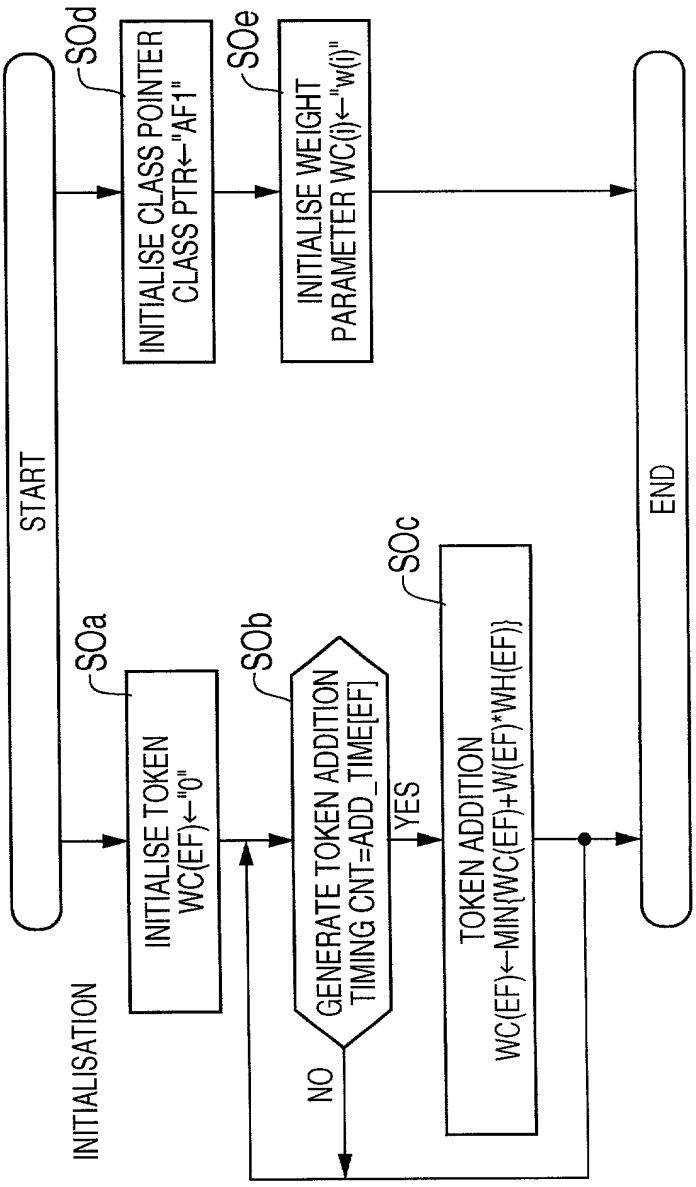
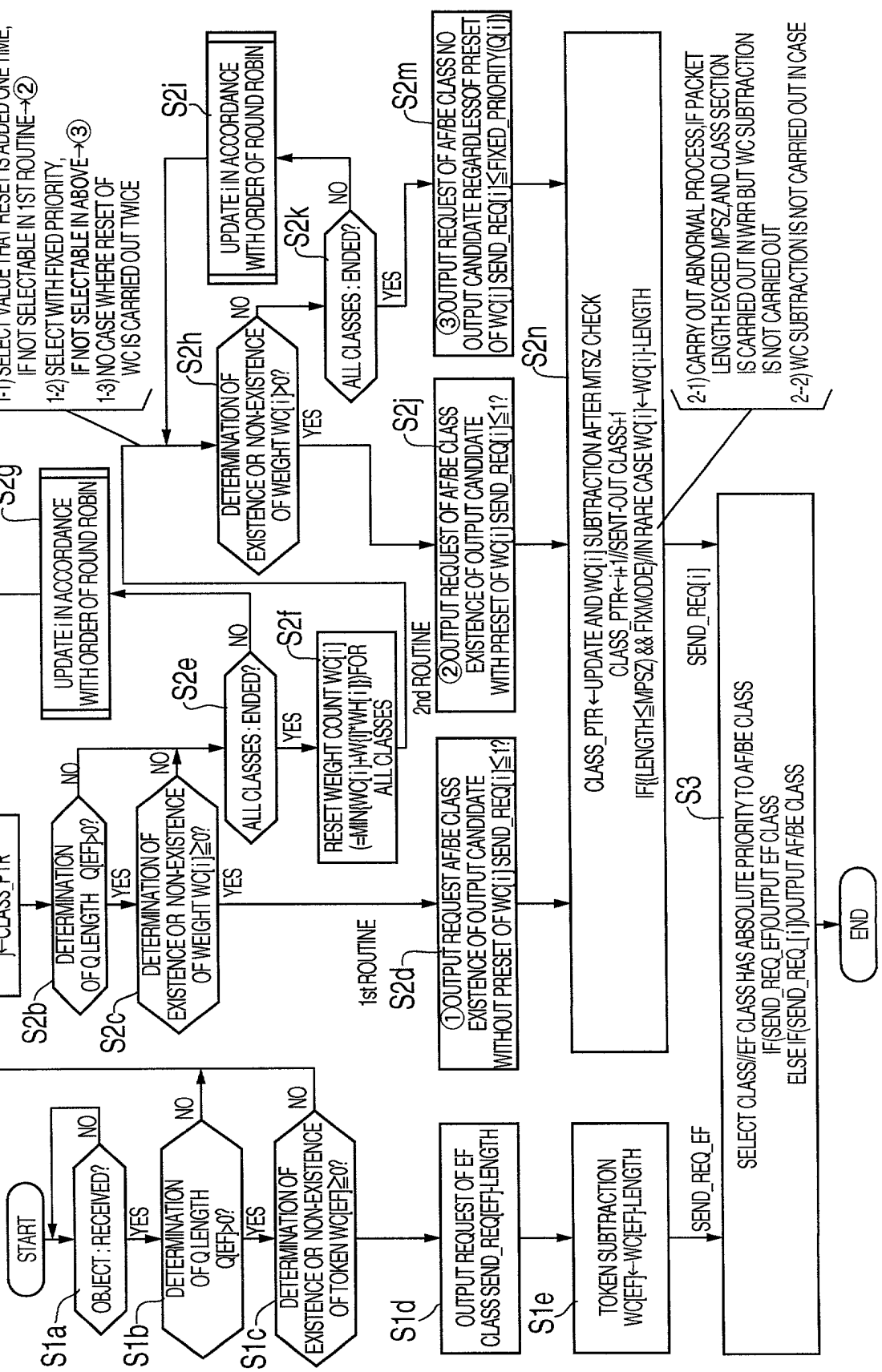

START
INITIALISATION
SOa
INITIALISE TOKEN
WC(EF)←"0"
SOb
GENERATE TOKEN ADDITION
TIMING CNT=ADD_TIME[EF]
NO
YES
SOc
TOKEN ADDITION
WC(EF)←MIN{WC(EF)+W(EF)*WH(EF)}
SOd
INITIALISE CLASS POINTER
CLASS PTR←"AF1"
SOe
INITIALISE WEIGHT
PARAMETER WC(i)←"w(i)"
END

Fig. 13


START
S1a
OBJECT : RECEIVED?
NO
YES
S1b
DETERMINATION OF Q LENGTH Q[EF]>0?
NO
YES
S1c
DETERMINATION OF EXISTENCE OR NON-EXISTENCE OF TOKEN WC[EF]≧0?
NO
YES
S1d
OUTPUT REQUEST OF EF CLASS SEND_REQ[EF]-LENGTH
S1e
TOKEN SUBTRACTION WC[EF]←WC[EF]-LENGTH
SEND_REQ_EF
S2a
j←CLASS_PTR
S2b
DETERMINATION OF Q LENGTH Q[EF]>0?
NO
YES
S2c
DETERMINATION OF EXISTENCE OR NON-EXISTENCE OF WEIGHT WC[i]≧0?
NO
YES
S2e
ALL CLASSES : ENDED?
NO
YES
S2f
RESET WEIGHT COUNT WC[i] (=MIN{WC[i]+W[i]*WH[i]})FOR ALL CLASSES
S2g
UPDATE i IN ACCORDANCE WITH ORDER OF ROUND ROBIN
1st ROUTINE
S2d
①OUTPUT REQUEST OF AF/BE CLASS EXISTENCE OF OUTPUT CANDIDATE WITHOUT PRESET OF WC[i] SEND_REQ[i]≦1?
2nd ROUTINE
S2h
DETERMINATION OF EXISTENCE OR NON-EXISTENCE OF WEIGHT WC[i]>0?
NO
YES
S2i
UPDATE i IN ACCORDANCE WITH ORDER OF ROUND ROBIN
S2k
ALL CLASSES : ENDED?
NO
YES
S2j
②OUTPUT REQUEST OF AF/BE CLASS EXISTENCE OF OUTPUT CANDIDATE WITH PRESET OF WC[i] SEND_REQ[i]≦1?
S2m
③OUTPUT REQUEST OF AF/BE CLASS NO OUTPUT CANDIDATE REGARDLESS OF PRESET OF WC[i] SEND_REQ[i]≦FIXED_PRIORITY(Q[i])
S2n
CLASS_PTR←UPDATE AND WC[i] SUBTRACTION AFTER MTSZ CHECK
CLASS_PTR←i+1//SENT-OUT CLASS+1
IF{(LENGTH≦MPSZ) && FIXMODE}//IN RARE CASE WC[i]←WC[i]-LENGTH
SEND_REQ[i]
S3
SELECT CLASS//EF CLASS HAS ABSOLUTE PRIORITY TO AF/BE CLASS
IF(SEND_REQ_EF)OUTPUT EF CLASS
ELSE IF(SEND_REQ_[i])OUTPUT AF/BE CLASS
END
1-1) SELECT VALUE THAT RESET IS ADDED ONE TIME, IF NOT SELECTABLE IN 1ST ROUTINE→②
1-2) SELECT WITH FIXED PRIORITY, IF NOT SELECTABLE IN ABOVE→③
1-3) NO CASE WHERE RESET OF WC IS CARRIED OUT TWICE
2-1) CARRY OUT ABNORMAL PROCESS,IF PACKET LENGTH EXCEED MPSZ,AND CLASS SECTION IS CARRIED OUT IN WRR BUT WC SUBTRACTION IS NOT CARRIED OUT
2-2) WC SUBTRACTION IS NOT CARRIED OUT IN CASE

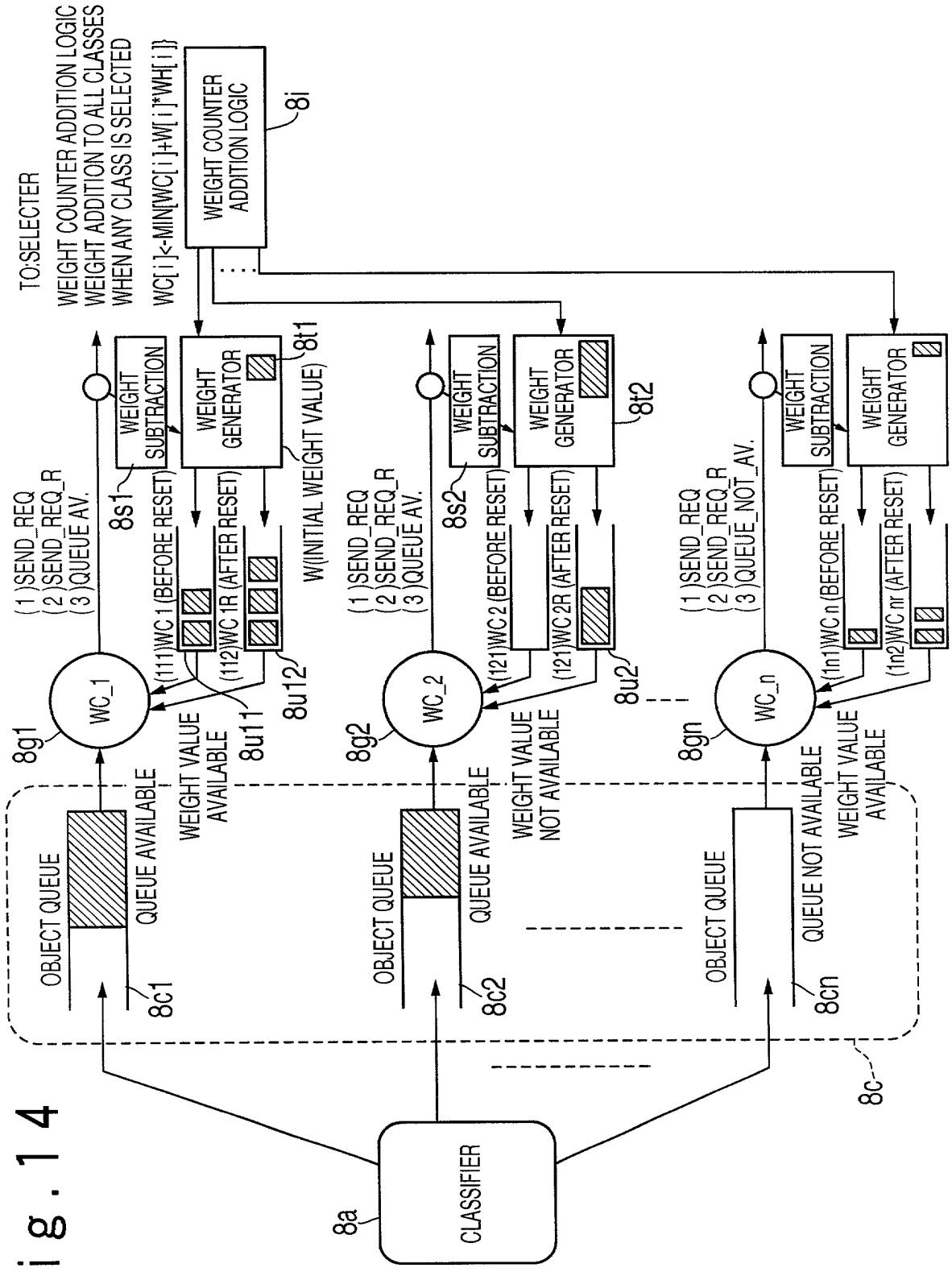

TO:SELECTER
WEIGHT COUNTER ADDITION LOGIC
WEIGHT ADDITION TO ALL CLASSES
WHEN ANY CLASS IS SELECTED
WC[i]<-MIN[WC[i]+W[i]*WH[i]]
WEIGHT COUNTER ADDITION LOGIC
8i
WEIGHT SUBTRACTION
WEIGHT GENERATOR
8t1
8s1
8t2
8s2
(1)SEND_REQ
(2)SEND_REQ_R
(3)QUEUE AV.
(3)QUEUE_NOT_AV.
(111)WC 1 (BEFORE RESET)
(112)WC 1R (AFTER RESET)
W(INITIAL WEIGHT VALUE)
(121)WC 2 (BEFORE RESET)
(121)WC 2R (AFTER RESET)
(1n1)WC n (BEFORE RESET)
(1n2)WC nr (AFTER RESET)
8u12
8u11
8u2
WC_1
WC_2
WC_n
8g1
8g2
8gn
WEIGHT VALUE AVAILABLE
WEIGHT VALUE NOT AVAILABLE
WEIGHT VALUE AVAILABLE
OBJECT QUEUE
QUEUE AVAILABLE
QUEUE NOT AVAILABLE
8c1
8c2
8cn
8c
CLASSIFIER
8a

Fig. 14

Fig. 15

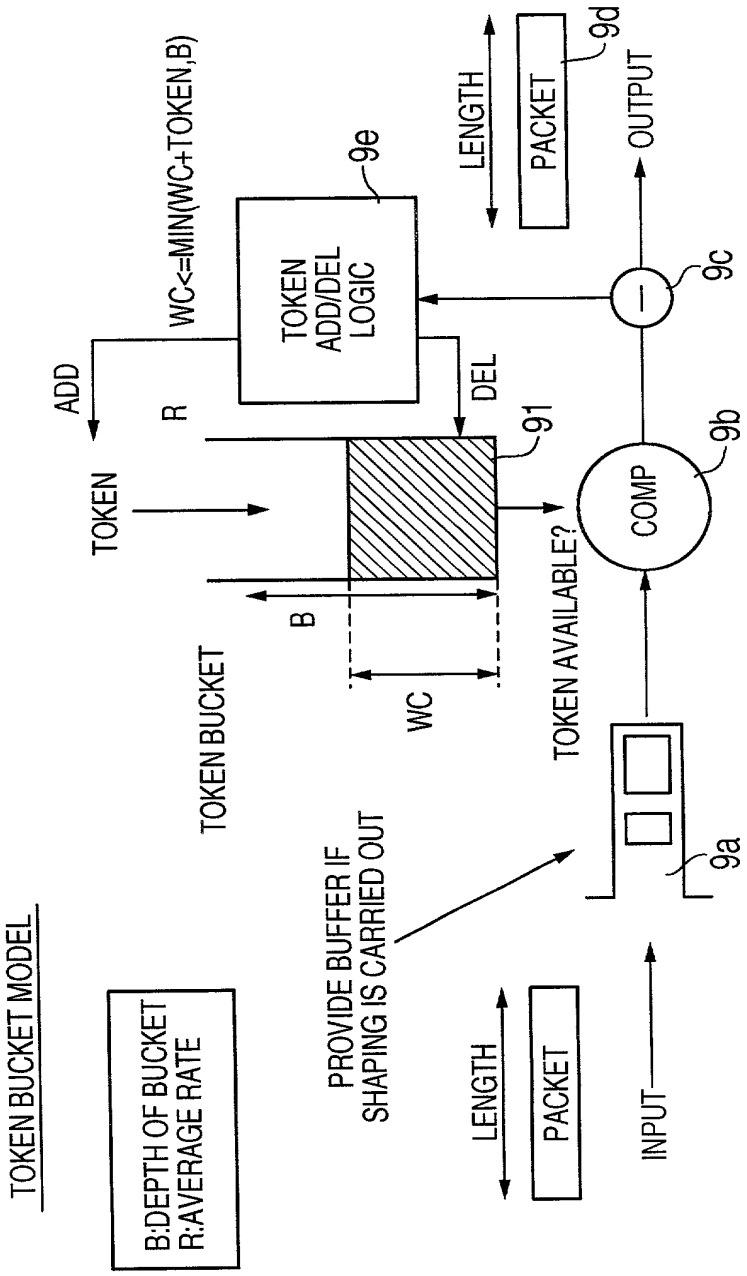
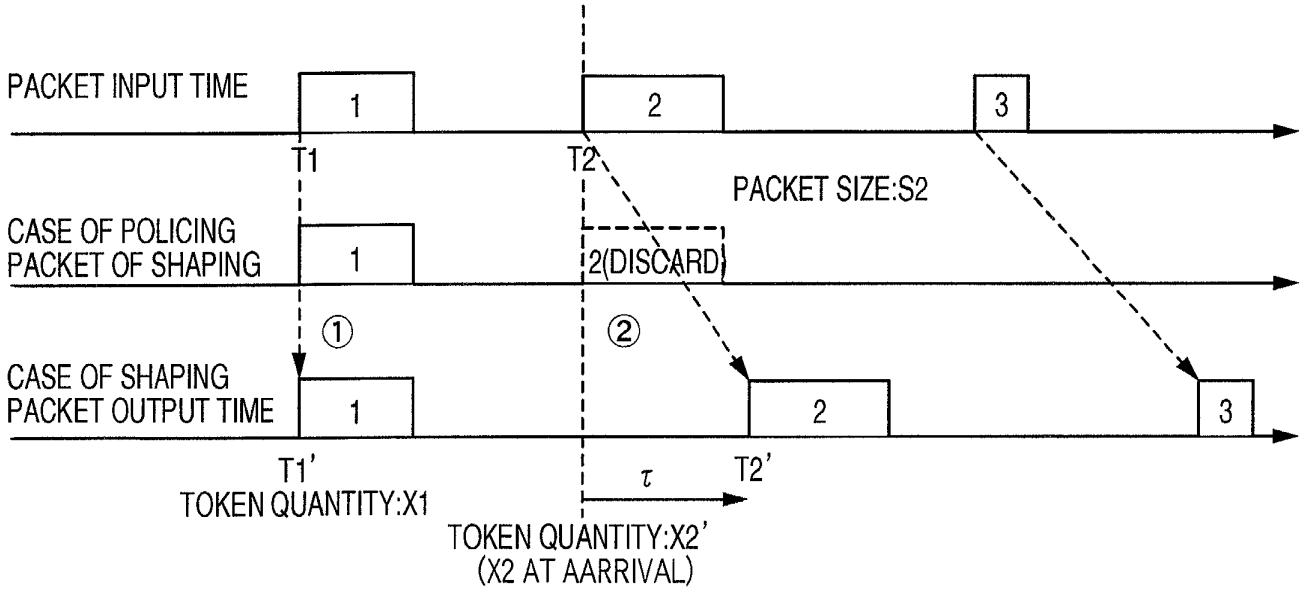

TOKEN BUCKET MODEL
B:DEPTH OF BUCKET
R:AVERAGE RATE
TOKEN BUCKET
TOKEN
ADD
R
B
WC
DEL
91
WC<=MIN(WC+TOKEN,B)
TOKEN ADD/DEL LOGIC
9e
PROVIDE BUFFER IF SHAPING IS CARRIED OUT
TOKEN AVAILABLE?
COMP
9b
9c
LENGTH
PACKET
9d
OUTPUT
INPUT
LENGTH
PACKET
9a

Fig.16



1)TOKEN QUANTITIY AT TIME T2:X2=x1+(T2-T1)*R
LACK OF TOKEN,IF S2>X2
2)POLICING
IMMEDIATELY DISCARD
3)SHAPING
NOT LACK OF TOKEN,IF PACKET IS TRANSMITTED AT TIME
(τ+T2)(S2=X1+{(τ+T2)-T1}*R).PACKET IS TRANSMITTED WITH DELAY τ